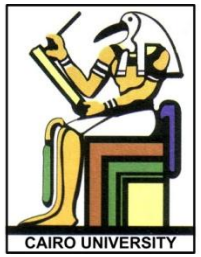


STM32 MICROCONTROLLER

Lecture 4

Prof. Yasser Mostafa Kadah

Nested Vectored Interrupt Controller

- The NVIC supports up to 56 maskable interrupt channels with 16 programmable priority levels
  - Not including the sixteen Cortex™-M3 interrupt lines
- NVIC and the processor core interface are closely coupled, which enables low latency interrupt processing and efficient processing of late arriving interrupts.
- The NVIC maintains knowledge of the stacked (nested) interrupts to enable tail-chaining of interrupts.

SysTick Calibration Value Register

- The SysTick calibration value is set to 9000, which gives a reference time base of 3 ms with the SysTick clock set to 3 MHz (max HCLK/8)

Interrupt and Exception Vectors

Table 50. Vector table for STM32F100xx devices

Position	Priority	Type of priority	Acronym	Description	Address
	-	-	-	Reserved	0x0000_0000
	-3	fixed	Reset	Reset	0x0000_0004
	-2	fixed	NMI_Handler	Non maskable interrupt. The RCC Clock Security System (CSS) is linked to the NMI vector.	0x0000_0008
	-1	fixed	HardFault_Handler	All class of fault	0x0000_000C

Interrupt and Exception Vectors

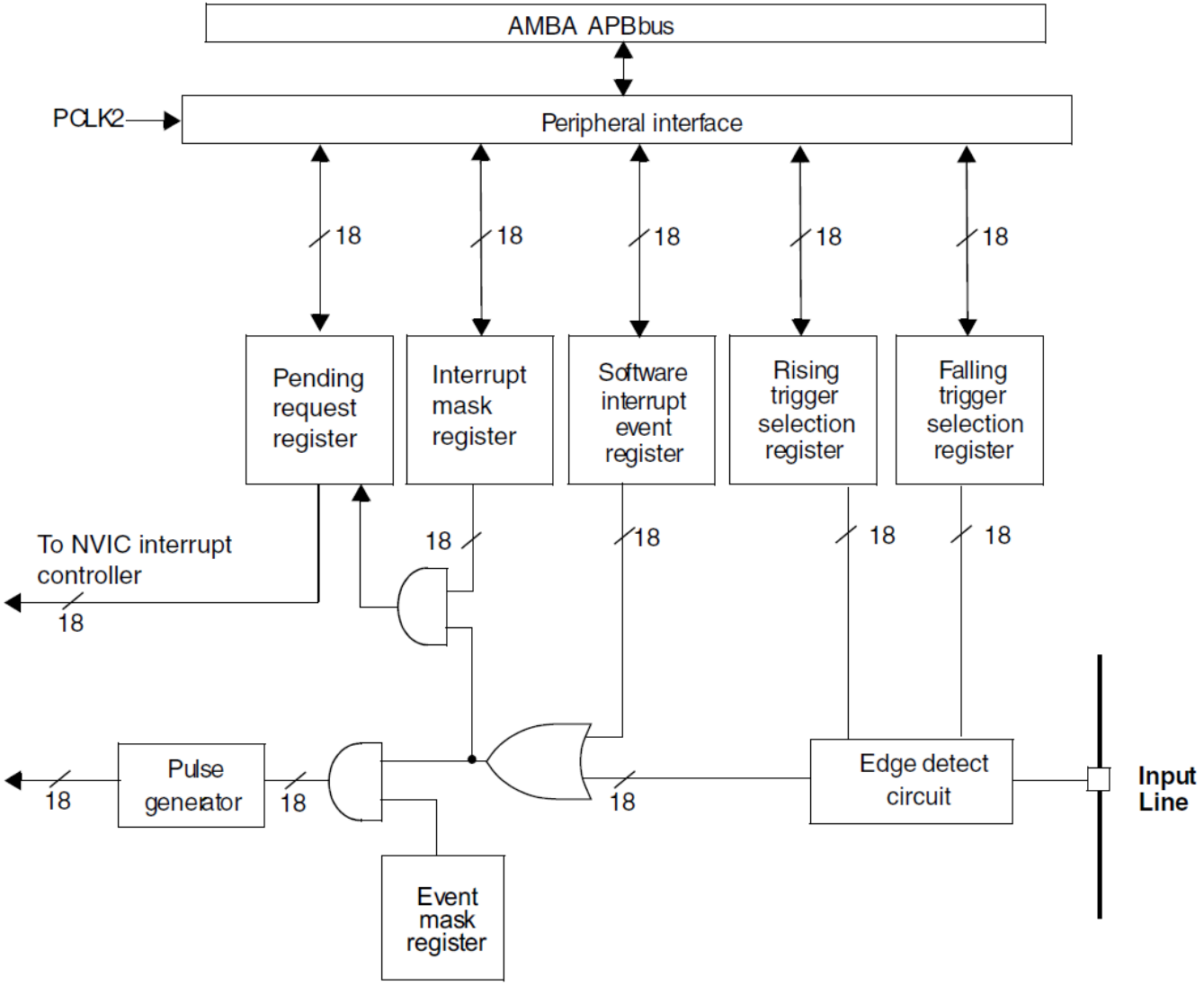
Table 50. Vector table for STM32F100xx devices (continued)

Position	Priority	Type of priority	Acronym	Description	Address
	0	settable	MemManage_Handler	Memory management	0x0000_0010
	1	settable	BusFault_Handler	Pre-fetch fault, memory access fault	0x0000_0014
	2	settable	UsageFault_Handler	Undefined instruction or illegal state	0x0000_0018
	-	-	-	Reserved	0x0000_001C - 0x0000_002B
	3	settable	SVC_Handler	System service call via SWI instruction	0x0000_002C
	4	settable	DebugMon_Handler	Debug Monitor	0x0000_0030
	-	-	-	Reserved	0x0000_0034
	5	settable	PendSV_Handler	Pendable request for system service	0x0000_0038
	6	settable	SysTick_Handler	System tick timer	0x0000_003C
0	7	settable	WWDG	Window Watchdog interrupt	0x0000_0040

External Interrupt/Event Controller (EXTI)

- Consists of up to 18 edge detectors for generating requests
- Each input line can be independently configured
  - Select the type (pulse or pending)
  - Select corresponding trigger event (rising or falling or both)
  - Each line can also be masked independently
- Pending register maintains the status line of interrupt requests
- EXTI controller main features are the following:
  - Independent trigger and mask on each interrupt/event line
  - Dedicated status bit for each interrupt line
  - Generation of up to 18 software event/interrupt requests

External Interrupt/Event Controller (EXTI)



NVIC Functional Description

- To generate the interrupt, the interrupt line should be configured and enabled.
- This is done by programming the two trigger registers with the desired edge detection and by enabling the interrupt request by writing a ‘1’ to the corresponding bit in the interrupt mask register.
- When the selected edge occurs on the external interrupt line, an interrupt request is generated.
- The pending bit corresponding to the interrupt line is also set. This request is reset by writing a ‘1’ in the pending register.

NVIC Functional Description

- To generate the event, the event line should be configured and enabled
- This is done by programming the two trigger registers with the desired edge detection and by enabling the event request by writing a ‘1’ to the corresponding bit in the event mask register
- When the selected edge occurs on the event line, an event pulse is generated and the pending bit corresponding to the event line is not set
- An interrupt/event request can also be generated by software by writing a ‘1’ in the software interrupt/event register

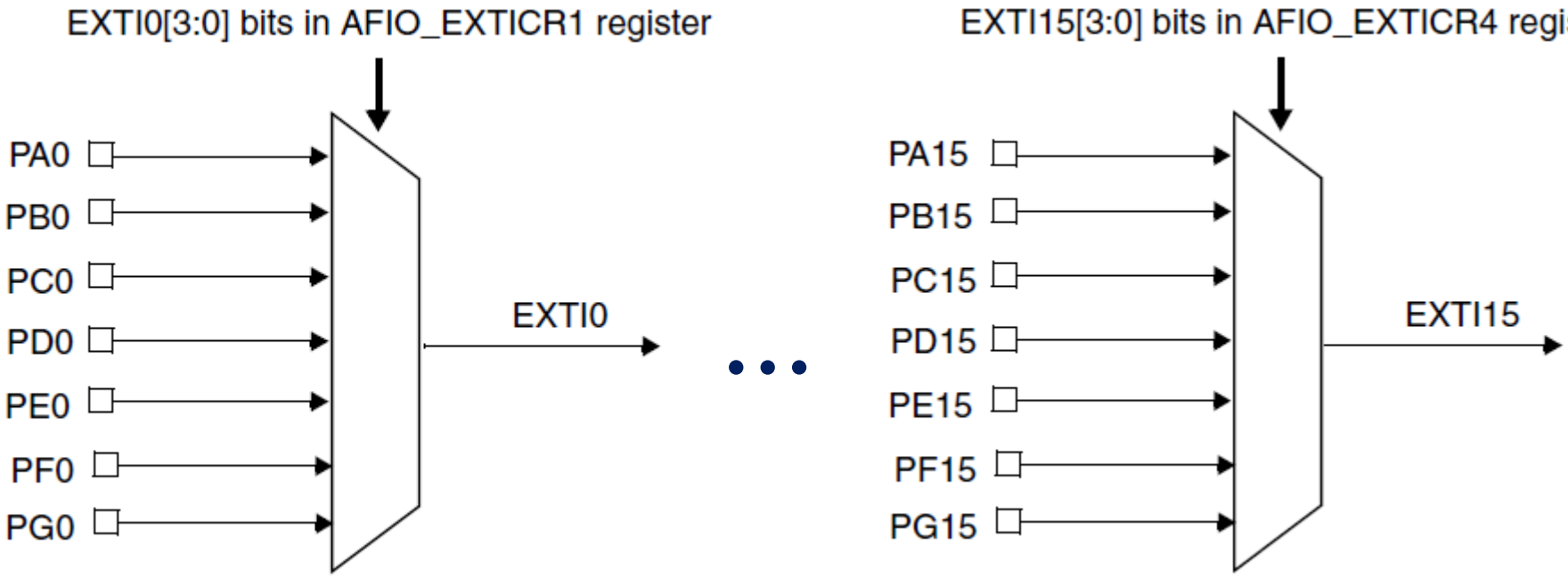
Hardware Interrupt/Event Selection

- To configure the 18 lines as interrupt sources, use the following procedure:
  - Configure the mask bits of the 18 Interrupt lines (EXTI_IMR)
  - Configure the Trigger Selection bits of the Interrupt lines (EXTI_RTSR and EXTI_FTSR)
  - Configure the enable and mask bits that control the NVIC IRQ channel mapped to the External Interrupt Controller (EXTI) so that an interrupt coming from one of the 18 lines can be correctly acknowledged
- To configure the 18 lines as event sources, use the following procedure:
  - Configure the mask bits of the 18 Event lines (EXTI_EMR)
  - Configure the Trigger Selection bits of the Event lines (EXTI_RTSR and EXTI_FTSR)

Software Interrupt/Event Selection

- The 18 lines can be configured as software interrupt lines as follows:
  - Configure the mask bits of the 18 Interrupt/Event lines (EXTI_IMR, EXTI_EMR)
  - Set the required bit of the software interrupt register (EXTI_SWIER)

External Interrupt/Event GPIO Mapping



- The two other EXTI lines are connected as follows:
  - EXTI line 16 is connected to the PVD output
  - EXTI line 17 is connected to the RTC Alarm event

Interrupt Mask Register (EXTI_IMR)

Address offset: 0x00
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														MR17	MR16
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:18 Reserved, must be kept at reset value (0).

Bits 17:0 **MRx:** Interrupt Mask on line x

0: Interrupt request from Line x is masked
1: Interrupt request from Line x is not masked

Event Mask Register (EXTI_EMR)

Address offset: 0x04
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														MR17	MR16
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:18 Reserved, must be kept at reset value (0).

Bits 17:0 **MRx:** Event mask on line x

0: Event request from Line x is masked
1: Event request from Line x is not masked

Rising trigger selection register (EXTI_RTSR)

Address offset: 0x08
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														TR17	TR16
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:18 Reserved, must be kept at reset value (0).

Bits 17:0 **TRx:** Rising trigger event configuration bit of line x

0: Rising trigger disabled (for Event and Interrupt) for input line
1: Rising trigger enabled (for Event and Interrupt) for input line

Falling trigger selection register (EXTI_FTSR)

Address offset: 0x0C
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														TR17	TR16
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:18 Reserved, must be kept at reset value (0).

Bits 17:0 **TRx:** Falling trigger event configuration bit of line x

0: Falling trigger disabled (for Event and Interrupt) for input line

1: Falling trigger enabled (for Event and Interrupt) for input line

Software Interrupt Event Register (EXTI_SWIER)

Address offset: 0x10
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														SWIER 17	SWIER 16
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWIER 15	SWIER 14	SWIER 13	SWIER 12	SWIER 11	SWIER 10	SWIER 9	SWIER 8	SWIER 7	SWIER 6	SWIER 5	SWIER 4	SWIER 3	SWIER 2	SWIER 1	SWIER 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:18 Reserved, must be kept at reset value (0).

Bits 17:0 **SWIERx:** Software interrupt on line x

Writing a 1 to this bit when it is at 0 sets the corresponding pending bit in EXTI_PR. If the interrupt is enabled on this line on the EXTI_IMR and EXTI_EMR, an interrupt request is generated.

This bit is cleared by clearing the corresponding bit of EXTI_PR (by writing a 1 into the bit)

Pending Register (EXTI_PR)

Address offset: 0x14
Reset value: undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														PR17	PR16
														rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PR15	PR14	PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

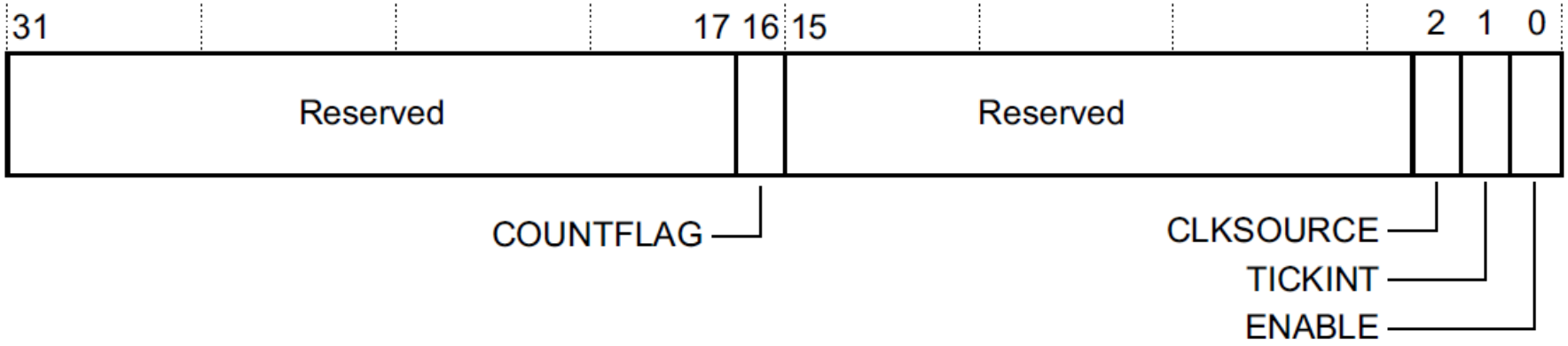
Bits 31:18 Reserved, must be kept at reset value (0).

Bits 17:0 **PRx:** Pending bit

0: No trigger request occurred
1: selected trigger request occurred
This bit is set when the selected edge event arrives on the external interrupt line. This bit is cleared by writing a 1 into the bit or by changing the sensitivity of the edge detector.

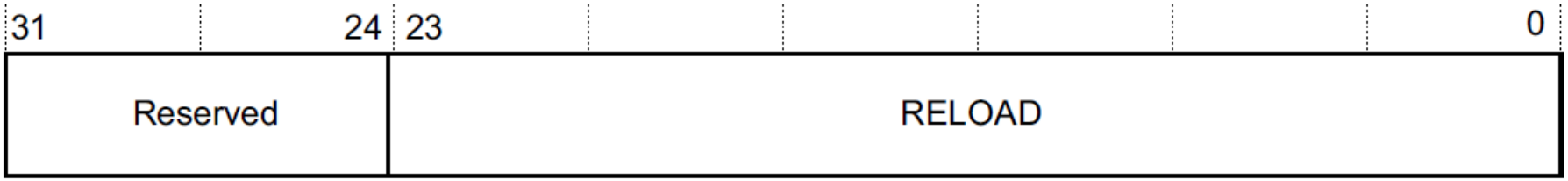
SysTick Control and Status Register

Address	0xE000E010
Access	Read/write
Reset state	0x00000000



SysTick Reload Value Register

Address	`0xE000E014`
Access	Read/write
Reset state	Unpredictable

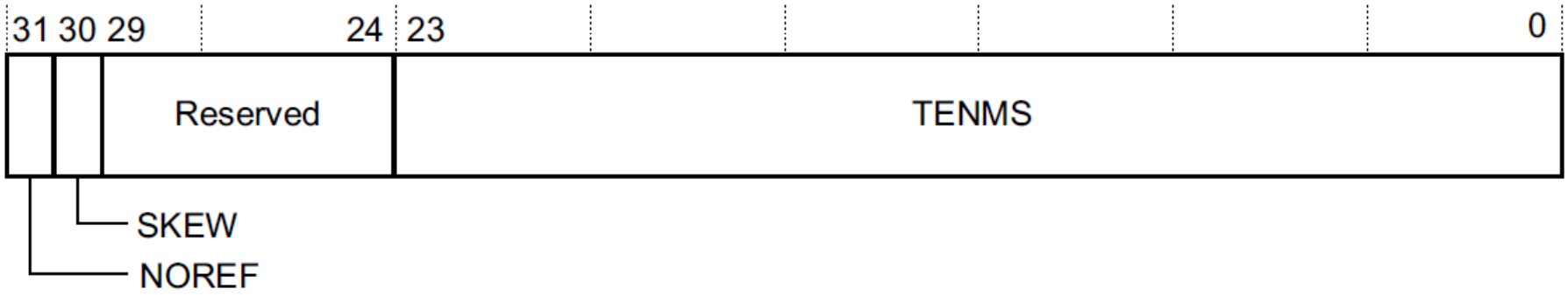


SysTick Current Value Register

Address	`0xE000E018`
Access	Read/write clear
Reset state	Unpredictable

SysTick Calibration Value Register

Address	0xE000E01C
Access	Read
Reset state	STCALIB



Assignments

- ARM Project #3