Embedded high-speed data acquisition and Digital Signal Processing platform for Digital Ultrasound Imaging

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Abstract

An embedded high-speed data acquisition and digital signal processing platform for digital ultrasound imaging is presented. In this work, the data acquisition and the digital signal processing algorithms are implemented on a low cost Xilinx Spartan 3E FPGA (Field Programmable Gate Array) chip. Echo signals received from the analog front-end are directed to the digital beam former on the FPGA. The A-scan line is obtained from the beam former which is then passes through a maximally flat FIR Hilbert transformer to yield a single side band of the A-scan to be band pass filtered. In order to achieve high speed acquisition compression techniques are involved. Large amounts of data are sent to the PC via high speed USB 2.0 interface. The huge amount of data sent to the PC allows for the employment of the prototype in developing ultrasound imaging devices with advancements of real time processing.

1. Introduction

Digital Ultrasound diagnostic devices have gained broad acceptance in a wide range of diagnostic fields because they are able to make observations inside the body safely and in real-time. An ultrasound device is comprised of a front-end segment for receiving the ultrasound signals, and a back-end segment that conducts signal processing and image processing to create images.

In the front-end, each echo signal received from a transducer element passes through a pre-amplifier, a time-gain amplifier (TGA), and converted into a digital signal by an A/D (Analog to Digital) converter. In the back-end, signals from different channels are then focused by a beam former to form a single A-scan line. The A-scan line is then processed, compressed and sent to the PC. Decompression and reconstruction then take place.

The following sections present (1) the design of a digital beam former to achieve high-resolution imaging, (2) real-time digital signal processing of the A-scan to produce an envelope of the signal, and (3) efficient lossless binary data compression of the envelope signal to enable the huge data transmission to the PC.

2. Digital Beamformer

Echo signals received from different crystals in the transducer array have different phases; these signals are aligned in phase by delay time control and are then added digitally to form the A-scan signal. This is called the delay-and-sum focusing. The circuit that makes this focusing is the beamformer. A high sampling rate, 100 MHz, of the A/D improves the delay resolution for the focusing in the beamformer.

3. Digital Signal Processing

The envelope of the A-scan is formed by first obtaining the single side band (SSB) of the signal. One copy of the signal is filtered using a maximally flat Hilbert transform block. Another copy is delayed by the same amount as the Hilbert module so both signal copies are synchronized. Both signals are also down sampled to the baseband or an intermediate frequency during this stage. The signals are then band pass filtered separately, and an envelope of the signal is formed by approximation using both copies of the signals. Logarithmic compression is then applied to control the dynamic range of the signals.

The maximally flat FIR filter is based on fractional Hilbert transform which is the generalization of the classical Hilbert transform but with improved performance. The maximally flat fractional Hilbert transform (MF FHT) approximates the ideal filter very well in the middle-frequency band. An efficient hardware realization structure is used to implement the maximally flat Hilbert transform based on the fact that any FIR filter can be expressed as a sum of symmetric and anti symmetric filter. This filter structure makes the number of multiplications

required for the filter implementation approximately equal to the traditional FIR min/max approximation. The frequency response is maximally flat in the pass band and experiences a relatively slow roll off. This frequency response specification is desirable for our signal narrow band specification. One important advantage of the MF FHT is that the impulse responses of odd order MF FHTs can be exactly expressed by fixed point binary values and implemented by the add and shift operations.

4. Binary Compression

Binary compression reduces the bit size of the A-scan. There are different lossless binary compression techniques that could be applied on the bitstream of data. Two techniques are proposed and are to be compared. The first is the Frequency Directed Run length code (FDR). It is a. variable-to-variable run length code based on encoding runs of 0' and runs of 1's of the bitstream. A sequence of symbols can be encoded using two elements for each run; the repeating symbol and the number of times it appears in the run. FDR is characterized by its insensitivity to variations in the input data stream. The second technique is based on numeric compression, using a Fibonacci numeric representation. A numeric succession (1, 3, 5, 8, 13...) is used as the weights of the bits of a binary string. It is used to evaluate the numeric value of the string instead of the binary succession (2^0, 2^1, 2^2, 2^3...). And then this numeric value is represented using the binary succession weights thus resulting in fewer bits.

5. Implementation

Some ultrasound systems use software to implement the beamformer, and digital signal processing algorithms, but the work presented uses hardware implementation to use the concept of "hardware acceleration" in which execution has a parallelism nature that speeds up the ultrasound system. Low-cost FPGA (Field Programmable Gate Array) is used for implementation of these algorithms as well as compression. The tools used in FPGA development and digital signal processing (DSP) are Xilinx ISE 10.1 Web-Pack, the DSP tools system generator, and MatlabR2007a.
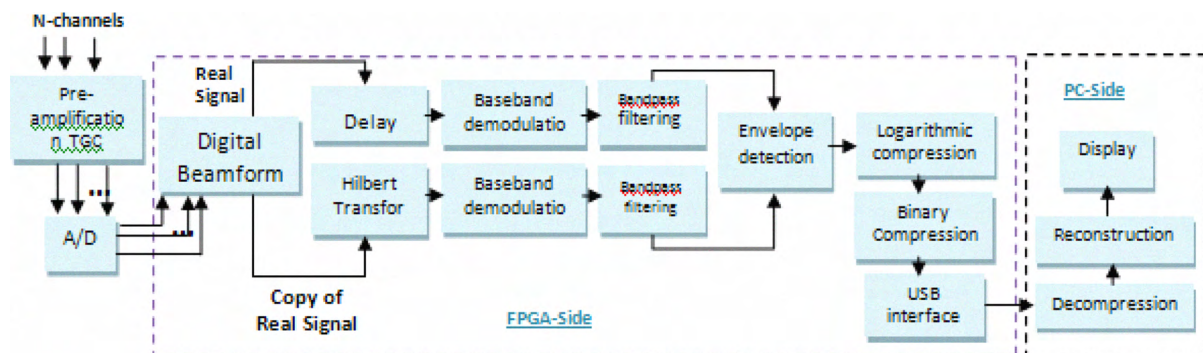
6. Conclusion

Flexibility and cost savings can be achieved with this work. FPGA circuits are programmable which makes it possible to add functions to the design or make modifications without changing the hardware. Fast, efficient algorithms and improved hardware architecture permit the modules to fit in one low-cost commercial FPGA.

References

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